A 5.7 GHz Hiperlan SiGe BiCMOS Voltage-controlled Oscillator and Phase-Locked-Loop Frequency Synthesizer

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Abstract – **A SiGe BiCMOS 5.5-6.4GHz frequency synthesizer is presented. The synthesizer consists of an oscillator with a phase noise of –110 dBc/Hz at 1 MHz offset, and a 10 GHz phase-lock-loop circuit with an in-band phase noise of -79 dBc/Hz. The power consumption of the ICs were 9 mW and 17mW, respectively.**

I. INTRODUCTION

In recent years, there has been a strong increase in wireless data and voice communication standards in various frequency bands. The U-NII and Hiperlan2 standards have allocated the 5.15-5.3 GHz and 5.470-5.725 GHz bands for wireless local area networks (W-LAN) in the United States and Europe, respectively. In order to meet the potentially high demand of such W-LAN products, low cost, highly integrated Si based transceivers are essential. The scope of this presentation is, therefore, to present a 6 GHz frequency synthesizer in a SiGe BiCMOS production technology which is suitable for a Hiperlan transceiver. To cover both frequency bands, the Voltage-Controlled Oscillator (VCO) should cover a relative wide frequency range of about 10%. The channel spacing of the standards are 20-23.5 MHz in order to realize high data-rates. Therefore, a PLL frequency step size of 1-5 MHz is mostly chosen in order to allow fast lock-in times and a low in-band phase noise of the channels.

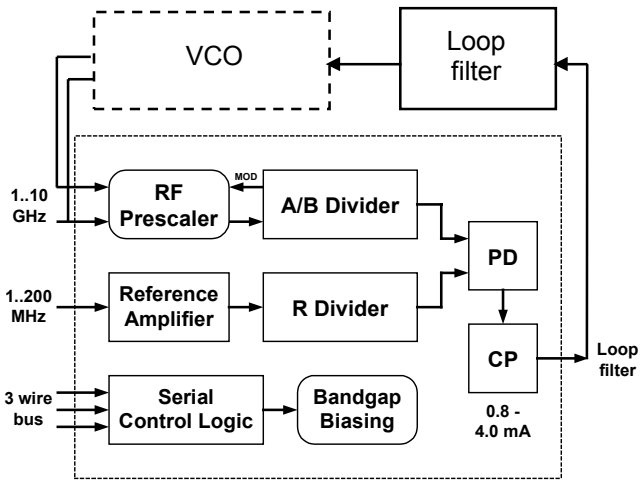

Fig. 1: Schematic diagram of the Hiperlan synthesizer

II. TECHNOLOGY

The 5.5-6.4 GHz VCO and the 10 GHz SiGe BiCMOS PLL were implemented in the commercially available Infineon B7HFC technology [1]. The technology offers high frequency (HF) and high voltage (HV) npn transistors, lateral and vertical pnp transistors, 1k and 50 Ω/sq. resistors, varactor diodes, MOS and MIM capacitors, electro-static-discharge (ESD) protection devices, and CMOS transistors with a gate length of 0.35um. The npn transistors have a transit frequency of 75 GHz, a maximum frequency of oscillation of 75 GHz and minimum noise figure of 0.9 dB at 2 GHz.

III. CIRCUIT DESIGN

The presented Hiperlan frequency synthesizer consists of a monolithically integrated 5.5-6.4 GHz VCO IC, a 10 GHz PLL IC, and a discrete Loop-filter (LPF) as shown in Fig. 1

A. Voltage-controlled oscillator design

The circuit design of the VCO is based on a previously presented 2.4 GHz bluetooth VCO [2]. Fig. 2 shows the schematic diagram of the VCO. The negative feedback of the VCO is generated by a capacitive cross-coupling of the collector and base terminals of a differential pair. The frequency of oscillation is determined by the LC parallel resonator at the collectors. The varactor diodes are differential devices, which leads to high quality factors of the fully differential VCO and an excellent pushing performance. The tuning range is determined by the capacitance ratio of the varactor diode for a tuning voltage of 0-3 V and the ac-coupling series capacitance. An ac-coupled emitter follower is used both to improve the pulling performance of the VCO and as a 50 Ω output driver. A layout of the VCO is shown in Fig. 3. The VCOs were packaged in a TSSOP-16 package.

B. Phase-locked-loop Synthesizer design

A block diagram of the PLL circuit and a die photograph is shown in Fig. 1 and 4, respectively. The PLL consists of a bipolar prescaler, programmable CMOS dividers for the RF (A/B) and the reference frequency (R), a CMOS phase detector (PD) and a programmable CMOS charge pump (CP). The dual-modulus prescaler consists of an input amplifier, a 4/5 divider, a 8/16 divider, output buffers and a

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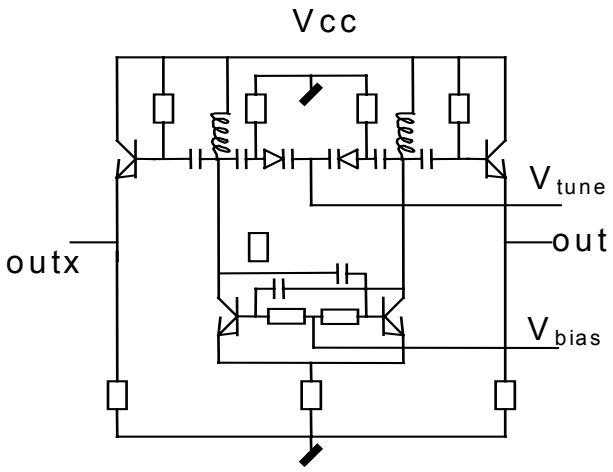

Fig. 2: Circuit diagram of monolithically integrated VCO

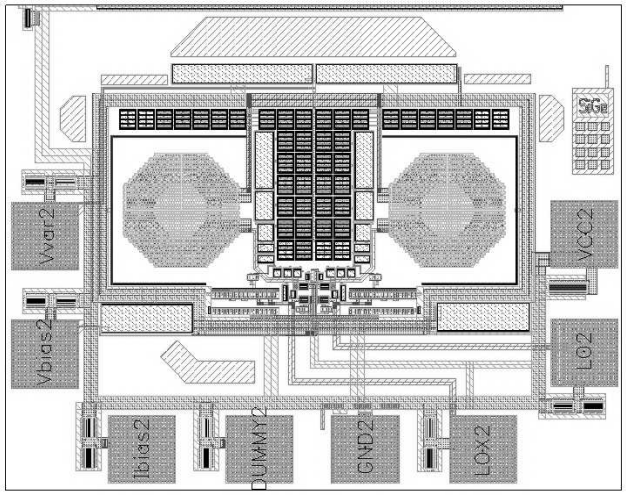

Fig. 3: Layout of the SiGe VCO

bandgap biasing circuit [3]. The logic blocks are implemented in differential current mode logic. The maximum operational frequency of the PLL is mostly determined by the speed of the 4/5 divider in the prescaler. The 4/5 divider consists of 3 D-type flip-flops in master-slave configuration operating at the input frequency. The RF frequency is determined by the 18 bit CMOS A/B divider, which generates the modulus signal for the prescaler. The frequency of the phase detector is determined by the programmable 12 bit reference frequency divider and the frequency of the reference quartz oscillator. A maximum reference frequency of 200 MHz can be applied. In order to achieve fast lock-in times of the PLL, phase detector frequencies of 1 to 5 MHz are mostly used for Hiperlan PLLs. A 2 bit programmable CMOS charge pump (0.8 to 4.5 mA) in combination with a discrete loop filter is used to generate the tuning voltage of the VCO.
The PLL is mounted in a 10-pin TSSOP package, and requires a supply voltage of 2.2 to 4.5 V.

IV. MEASUREMENTS AND RESULTS

A. Voltage-controlled oscillator results

The spectrum of the VCO is shown in Fig. 5. For this measurement, the VCO was locked at 6 GHz with the PLL and the out-band phase noise was measured. The measured value of –110 dBc/Hz at 1 MHz offset is sufficient for the Hiperlan standard and is 9 dB lower than recently reported 5 GHz frequency synthesizers [4]-[5]. The measured phase noise performance in combination with low VCO power consumption of 9 mW demonstrates a state-of-the-art performance for monolithically integrated 6 GHz VCOs [6].
Fig. 6 shows the tuning characteristics of the VCO at a supply voltage of 3 V. A tuning range from 5.5 to 6.4 GHz is obtained, i.e. a variation of 15%. In combination with the low phase noise, this is an outstanding tuning range for the integrated VCO. Since a maximum variation of 255 MHz is required within each frequency band, the presented VCO has sufficient margins for production tolerances. The VCO frequency can be easily centered to the required frequency by re-sizing the varactor area or reducing the ac-coupling capacitors. Fig 5 also shows that the frequency gain k_{VCO}, i.e. the change of the oscillation frequency of the VCO versus the tuning voltage, has an excellent linear behavior with tuning sensitivities of 250-450 MHz/V. Within a maximum Hiperlan tuning range of 255 MHz the tuning sensitivity varies only by ±15%. This linearity is significantly better than previously reported 5 GHz VCOs [4]-[5] and enables an accurate loop-filter design for fast lock-in times of the Hiperlan frequency synthesizer.
Fig. 7 shows the VCO phase noise and single-ended output power versus the VCO core current at 3 V. The best phase noise is obtained for a core current of 5 mA, which corresponds to an output power of -9.5 dBm.

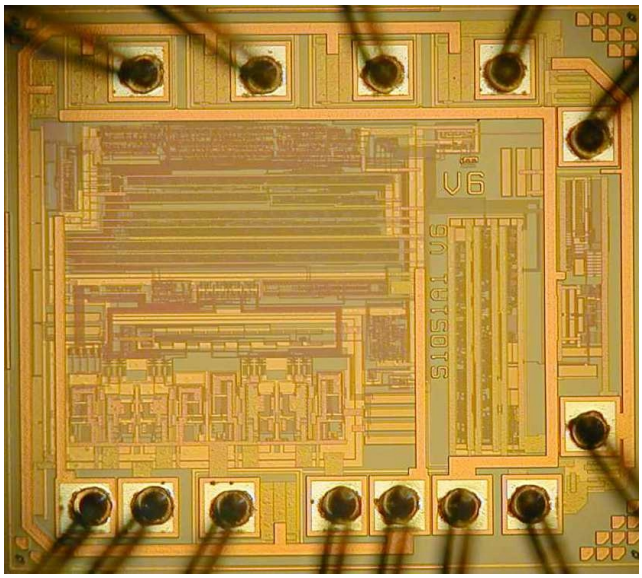

Fig. 4: Chip photograph of the SiGe BiCMOS PLL

B. Phase-locked-loop Synthesizer results

Fig. 8 shows the in-band phase noise of the frequency synthesizer at 6 GHz. A phase noise of –79 dBc was measured for a phase detector frequency of 1 MHz and a reference frequency of 10 MHz. This value is sufficient for a Hiperlan frequency synthesizer. A lower in-band phase noise can be generally obtained using a higher reference frequency or a higher phase detector frequency. As a figure of merit for the PLL a noise floor of -214 dBc/Hz is, therefore, calculated from the measured phase noise. This value is comparable to present mobile phone PLLs at 1-2 GHz and demonstrates the excellent high speed and low phase noise performance of the SiGe PLL.

Fig. 5 further shows the spurious performance of the PLL. No spurious peak can be measured at the phase detector frequency of 1 MHz, which results in a spurious suppression of better than –70dBc/Hz. This value is more than 20 dB better than recently reported SiGe BiCMOS [4] and CMOS [5] 5 GHz synthesizers and demonstrates the linear phase detector characteristics and the low leakage current of both the CMOS charge pump and VCO varactor diode. A PLL loop bandwidth of 100 kHz is chosen in order to enable fast lock-in times.

Fig. 9 shows the in-band phase noise and spurious suppression of the PLL for different charge pump tuning voltages at a supply voltage of 3V. Generally the charge pump currents are reduced if the voltage drop over the current sources is below the threshold voltage. As a result, a spurious peak, resulting in a reduced spurious suppression is observed at charge pump voltages below 0.5V and above 2.4V (V_{dd}-0.6V). However, the phase noise performance is not degraded as significantly, resulting in a larger operational range of 0.3V to 2.6V (V_{dd}-0.3V) for the charge pump output voltage.

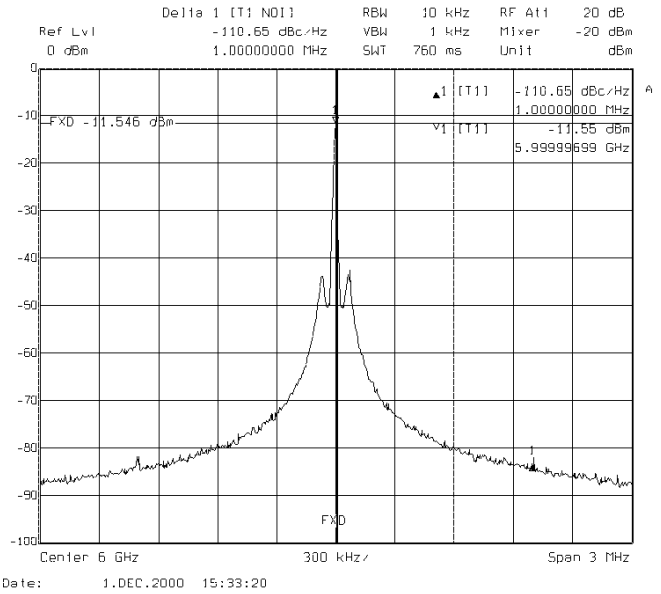

Fig. 5: VCO phase noise spectrum at 2.2V and 4mA core current

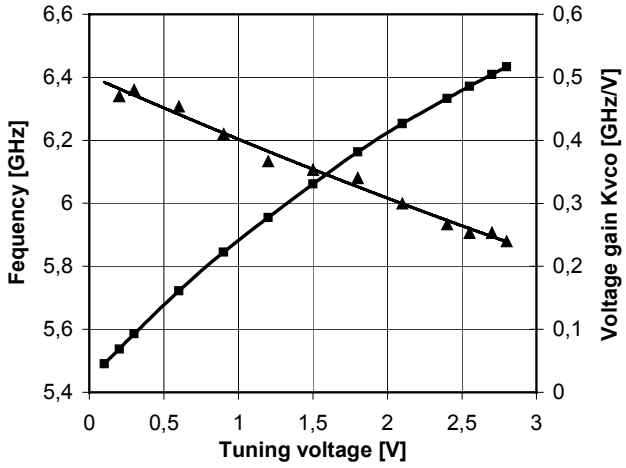

Fig. 6: Tuning charcteristics of the VCO

Fig. 10 shows the PLL performance for different supply voltages. An in-band phase noise below –78 dBc was obtained for supply voltages above 2.4 V. The minimum supply voltage is limited by the integrated bandgap circuit which is used for the biasing of the bipolar dividers. The spurious suppression is found to be independent of the PLL supply voltage from 2.2 to 4.5 V. This demonstrates the excellent symmetry of the charge pump sink and source currents of charge pump. For Hiperlan applications were lowest power consumption is required, a supply voltage of 2.2 V is recommended for the presented VCO and PLL ICs.

Fig. 11 shows the measured input sensitivity of the PLL. At 6 GHz an input power of –20 dBm to +10 dBm is required. Fig. 11 further shows a maximum operational frequency of 10.5 GHz, which is, to our knowledge, the highest reported PLL frequency for SiGe BiCMOS PLLs. The power consumption of the PLL is only 17 mW, i.e. 7.6 mA at

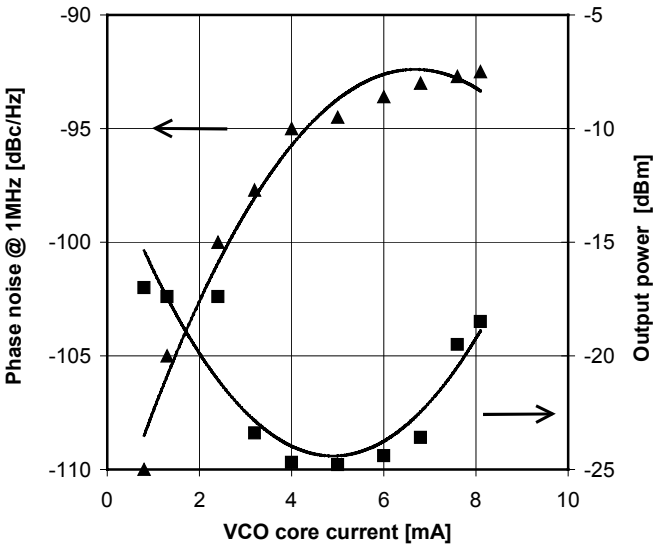

Fig. 7: VCO Performance vs. VCO core current at 3 V

2.2V, which is significantly lower than previously reported 5 GHz PLLs [4]-[5] and demonstrate the state-of-the-art speed-power performance of the SiGe BiCMOS technology.

V. CONCLUSION

A SiGe BiCMOS Hiperlan frequency synthesizer is presented. The TSSOP-16 packaged 5.5-6.4GHz VCO shows a phase noise of –110 dBc/Hz at 1 MHz offset with a power consumption of 9 mW. The TSSOP-10 packaged PLL shows a maximum frequency of 10 GHz, an in-band phase noise of –79 dBc, a spurious suppression of –70 dBc with a power consumption of 17 mW. These state-of-the-art results demonstrate that SiGe BiCMOS is an excellent technology for mobile communication ICs.

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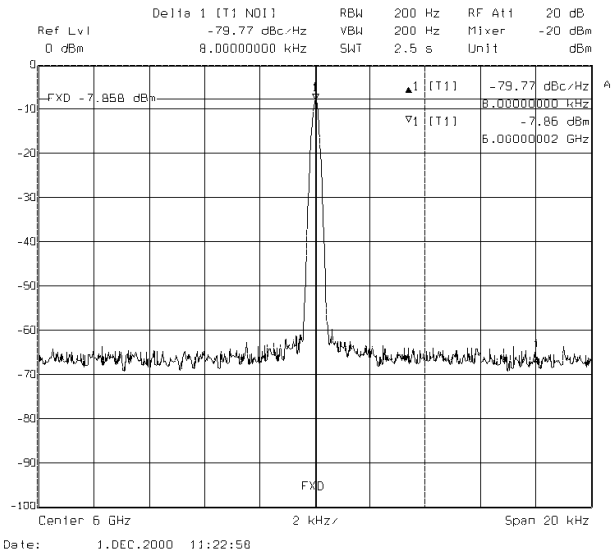

Fig. 8: In-band phase noise spectrum of the SiGe PLL

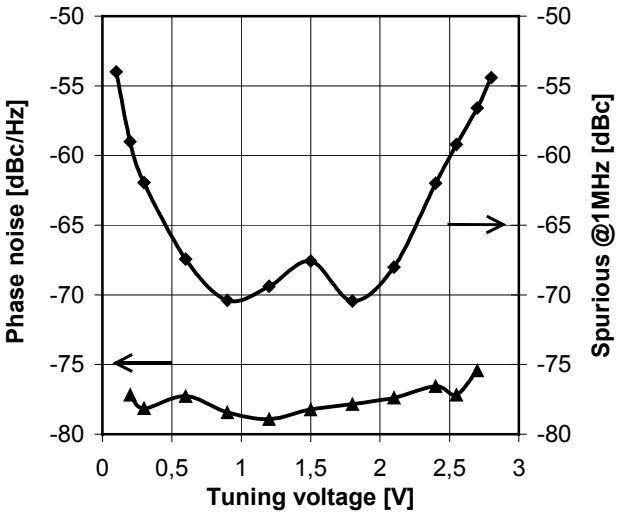

Fig. 9: PLL performance vs. charge pump voltage

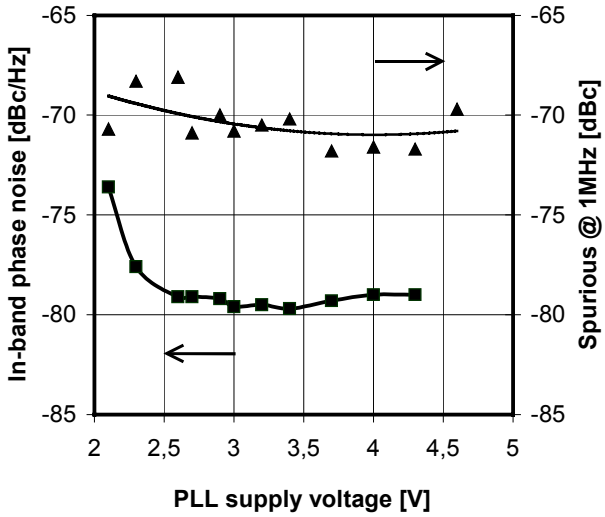

Fig. 10: PLL performance vs. supply voltage

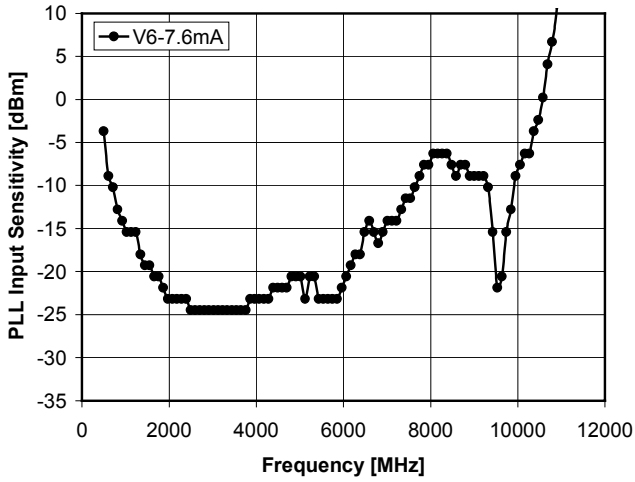

Fig. 11: PLL input sensitivity at Vcc=2.7V and I=7.6mA